Amendments to the Specification:

Please amend lines 1-12, page 1 (Background Of The Prior Art) with the following amended paragraph:

Prior to commencing comprehensive image data processing, which may include [[e.g.,]] searching for symbol or character representations, decoding and character recognition processing, presently available optical readers clock out and capture in a memory location at least one exposure test frame of image data, read pixel data from the memory-stored exposure test frame to determine an exposure parameter value that is based on actual illumination conditions, then utilize the exposure parameter value in the exposure of a frame of image data that is clocked out, and then subjected to searching, decoding, and/or character recognition processing. The frame of image data exposed utilizing the exposure parameter based on actual illumination conditions is not available for reading until after it is clocked out. Presently available optical readers therefore exhibit an appreciable inherent exposure parameter determination delay. Readers having higher resolution imagers have slower frame clock out rates and therefore longer exposure parameter determination delays.

Please amend lines 1-8, page 5 with the following amended paragraph:

A reader configured in accordance with the invention clocks out and captures in a memory storage location at least one parameter determination frame of image data in a "low resolution" frame capture mode, reads pixels of the parameter determination frame in establishing at least one operation parameter that is based on actual illumination conditions, utilizes the determined operation parameter in clocking out a subsequent frame of image data in a "normal resolution mode," then captures and subjects the frame of image data clocked out utilizing the operation parameter to image data searching, decoding, and/or recognition processing. The reader may be adapted to decode a decodable symbol represented in a frame of image data developed utilizing a determined operating parameter.

Please amend lines 15- 26, page 7 and lines 1-6, page 8 with the following amended paragraph:

Optical reader 10 of Fig. 2a also includes programmable control circuit 40 which preferably comprises an integrated circuit microprocessor 42 and an application specific integrated circuit (ASIC 44). The function of ASIC 44 could also be provided by field ~~programable~~ programmable gate array (FPGA). Processor 42 and ASIC 44 are both programmable control devices which are able to receive, output and process data in accordance with a stored program stored in memory unit 45 which may comprise such memory elements as a read/write random access memory or RAM 46 and an erasable read only memory or EROM 47. RAM 46 typically includes at least one volatile memory device but may include one or more long term non-volatile memory devices. Processor 42 and ASIC 44 are also both connected to a common bus 48 through which program data and working data, including address data, may be received and transmitted in either direction to any circuitry that is also connected thereto. Processor 42 and ASIC 44 differ from one another, however, in how they are made and how they are used.

Please amend lines 17-26, page 9 and lines 1-12, page 10 with the following amended paragraph:

Processor 44 is preferably devoted primarily to controlling the image acquisition process, the A/D conversion process and the storage of image data, including the ability to access memories 46 and 47 via a DMA channel. Processor 44 may also perform many timing and communication operations. Processor 44 may, for example, control the illumination of LEDs 22, the timing of image sensor 32 and an analog-to-digital (A/D) converter 36, the transmission and reception of data to and from a processor external to reader 10, through an RS-232, a network such as an ~~ethernet~~, Ethernet a serial bus such as USB, a wireless communication link (or other) compatible I/O interface 37. Processor 44 may also control the outputting of user perceptible data via an output device 38, such as a beeper, a good read

LED and/or a display monitor which may be provided by a liquid crystal display such as display 82. Control of output, display and I/O functions may also be shared between processors 42 and 44, as suggested by bus driver I/O and output/display devices 37′ and 38′ or may be duplicated, as suggested by microprocessor serial I/O ports 42A and 42B and I/O and display devices 37" and 38′. As explained earlier, the specifics of this division of labor is of no significance to the present invention.

Please amend lines 24-26, page 12 and 1-8, page 13 with the following amended paragraph:

Fig. 1a shows a schematic diagram of an exemplary image map frame that is clocked out according to the low resolution frame clock out mode of the invention and then captured into memory 45. The image map is divided into "zones" of valid data and invalid data. Valid zones 84 shown are rows of pixels that are clocked out at a normal clock out speed while invalid zones 86 shown are rows of ~~pixel~~ pixels that are clocked out at a faster clock out speed, which is normally (but not necessarily) a speed insufficient to allow development of electrical signals accurately representing the intensity of light at a pixel.

Please amend lines 21-26, page 13 and line 1-6, page 14 with the following amended paragraph:

Using CMOS fabrication techniques, image sensors are readily made so that electrical signals corresponding to certain pixels of a sensor can be selectively clocked out without clocking out electrical signals corresponding to remaining pixels of the sensor. CMOS image sensors are available from such manufacturers as Symagery, Pixel Cam, Omni Vision, Sharp, Natural Semiconductor, Toshiba, Hewlett-Packard and Mitsubishi. Further aspects of a partial frame clock out mode are described in commonly assigned ~~application Serial~~ Application No. ~~————~~ 09/766,806 entitled "Optical Reader Having Partial Frame Operating Mode[[,]] " now U. S. Patent No. 6,637,658 filed concurrently herewith and incorporated herein by reference.

Please amend lines 5-18, page 15 with the following amended paragraph:

At time T1, control circuit 40 activates a frame clocking signal to commence the clock out a first frame of pixel data according to a normal resolution frame clock out mode[[ ]] (the pixel data clocked out during clock out period CP1 is normally invalid pixel data). During clock out period CP1, the charges built up on pixel array 32a during clock out period CP0 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP1 pixel array 32a is exposed to light for a time determined by an exposure parameter value, e_0, that was previously transmitted at time Te_0 prior to time T1. The exposure parameter e_0 is based on previous exposure values during a previous trigger actuation period or based on expected illumination conditions, but is not based on actual illumination conditions present.

Please amend lines 15-26, page 17 through lines 1-20, page 18 with the following amended paragraph:

At time T3, control circuit 40 activates a frame clock out signal to commence the capture of a third frame of image data in accordance with a normal resolution frame clock out mode. During clock out period CP3, the charges built up on pixel array 32a during clock out period CP2 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP3, pixel array 32a is exposed to light for a time determined by an exposure parameter value, e_2, that was previously transmitted at time Te_2 prior to time T3. Unlike the previous exposure values e_0 and e_1, the exposure parameter value e_2 can be a value determined from actual illumination conditions since the frame of image data resulting from pixel array 32a being exposed to light during clock out period CP1, is available for reading by control circuit 40 prior to the time that the exposure parameter e_2 must be communicated to image sensor 32. However, because of the built in one frame delay resulting from the presence of buffer 32b, it is seen that a frame of image data clocked out while being exposed with the exposure parameter value e_2, determined based on actual

illumination conditions, will not be available for reading by control circuit unit after the expiration of clocking period CP4. Accordingly, it can be seen that the above reader exhibits a typical parameter determination delay of four normal resolution clock out periods, CP1+CP2+CP3+CP4 plus the frame discharge clock out parameter CP0. The normal resolution frame clock out ~~rate~~ period of the above-referenced SONY image sensor is about 33.37 ms and the frame discharge ~~rate~~ period is about 8.33 ms, resulting in a typical-case total parameter determination delay in the example described of 140ms (an earlier frame may be subjected to image data searching, decoding, and recognition if e_0 or e_1 yields an image of acceptable quality).

Please amend lines 21-26, page 18 and lines 1-21, page 19 with the following amended paragraph:

Advantages of operating image sensor 32 according to a low resolution frame clock out mode of operation are easily observable with reference to time line 94 corresponding to a reader having an image sensor operated in accordance with a low resolution frame clock out mode. In the example illustrated by time line 94 control circuit 40 operates image sensor as described in connection with Fig. 3b except that control circuit 40 operates image sensor 32 according to a low resolution frame clock out mode during clocking periods CP1, CP2, and CP3. Because electrical signals corresponding to only some of the pixels during these timing periods are clocked out at speeds sufficiently slow to read valid image data, the total frame clock out time ~~association~~ associated with these clocking periods is significantly shorter than that of a frame clocked out according to a normal resolution frame clock out mode. In an exemplary embodiment in which control circuit 40 alternatingly changes the state of a discharge clock out control signal (known as an EFS signal) in communication with a SONY ICX084AL CCD image sensor, to result in a zone division pattern having valid zones comprising four pixel rows clocked out at normal speed bounded by invalid rows having eighteen rows of pixels ~~clock~~ clocked out at high speed, the low resolution frame clock out rate is 8.52 ms. The overall typical parameter determination delay is therefore reduced to

T0+T1+T2+T3+T4=66.2 ms as compared to the 140 ms delay in the prior art reader example described with reference to Fig. 3a.

Please amend lines 15-26, page 20 and lines 1-4, page 21 with the following amended paragraph:

Additional reader operating parameters can be determined by reading pixel values from a frame of image data clocked out according to a low resolution clock out mode of the invention. These additional parameters which may be determined from a low resolution parameter determining frame of image data include an amplification parameter for adjusting the gain of an amplifier prior to analog-to-digital conversion, an illumination level parameter for adjusting the current level delivered to, and therefore the radiance of light emitted from LEDs 22, an illumination time parameter for adjusting the on-time of LEDs 22, a light level parameter for adjusting a light level[[,]] of a subsequently captured frame of image data, a dark level parameter for adjusting a dark level, of a subsequently captured frame of image data, and an ~~analog-to-digital~~ analog-to-digital converter reference parameter for adjusting a reference voltage of analog-to-digital converter 36.